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OPTIMIZATION OF a-Si SOLAR CELL CURRENT COLLECTION

Y. Gupta, H. Liers, S. Woods, S. Young
Science Applications, Inc.
1710 Goodridge Drive
McLean, VA 22102

R. DeBlasio, L. Mrig
Solar Energy Research Institute
1617 Cole Boulevard
Golden, CO 80401

ABSTRACT

This paper develops a quantitative methodology to evaluate power losses resulting from current collection in a-Si:H modules. Analytic expressions are derived for optimum cell width and grid spacing as a function of design parameters for series cells with and without metallic collection grids. Current collection losses can be reduced to about 2% using optimized designs with fairly narrow cell widths of less than a centimeter. The methodology can also be used to evaluate power losses for other thin film technologies such as CdS.

INTRODUCTION

The develoment of amorphous silicon (a-Si) solar cells is one of the most promising avenues of investigation in the pursuit of low cost photovoltaic power technologies. Recent advancements have led to increasingly efficient a-Si:H cells and improved understanding of manufacturing techniques and theoretical mechanisms. Module design requirements and tradeoffs, however, have not yet been evaluated extensively. Recently, Science Applications, Inc. (SAI) performed a study for the Solar Energy Research Institute (SERI) to investigate module design techniques and develop design concepts. This paper addresses one important issue which is the design of the cell current collection configuration, including analysis and optimization of the associated resistive power losses and cell area losses.

MODULE DESIGN CONSIDERATIONS

Effective module design concepts will utilize a monolithic cell/module structure to take advantage of the mass production capabilities and cost reduction potential of the a-Si:H thin film material. The module structure may include a glass or other structural and protective encapsulant; anti-reflective coatings; a current collection layer using TCO and/or metallic grids; the actual cell device layers including the p^+-doped a-Si:H layer, the i layer, and the n^+ layer; a reflective back surface; and a protective or structural substrate. The p^+, i, n^+ layers can also be reversed in order from the direction of incident light to form an n^+, i, p^+ device. Some form of both encapsulant and substrate is required to provide protection from the environment, and at least one must also provide structural support. The reflective back surface is added to improve efficiency by reflecting light transmitted through the thin layers of the device.

CELL CURRENT COLLECTION CONFIGURATIONS

An analysis of cell current collection and interconnection design was performed for two configurations: (1) surface current is carried by a transparent conductive oxide (TCO) layer only; and (2) surface current is carried by both TCO and metallic grid fingers. Conceptual schematics for the two configurations are shown in Figures 1 and 2. In both configurations shown the cells are connected in series, although it would also be possible to evaluate other arrangements. The individual "cells" with interconnections and insulated gaps between them are created by laser

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or masking techniques from a single large-area manufacturing process. As shown in the figures, the current flows through the a-Si:H cell semiconductor junction, gets collected by the TCO layer, is conducted either through the TCO layer or the metal grid fingers to the metal interconnect, and finally is conducted to metal substrate and back to the next cell in series. The analysis below is performed using representative values of the cell and process parameters.

FRACTIONAL LOSS COMPONENTS

Losses associated with the current collection configuration include:

- cell area losses resulting from gaps
- cell area losses resulting from shading
- surface resistive losses in the TCO collection layer
- bulk resistive losses
- contact resistive losses
- metal resistive losses.

To provide a basis for comparison, losses are expressed on a fractional basis. The fractional loss is defined as

$$(1)\quad F = P_{loss}/P_{max}$$

where P_{loss} represents the total power losses relating to current collection for a unit cell area, and P_{max} is the maximum theoretical power which could be delivered to the load from the unit cell area if no current collection (i.e., resistive and cell area) losses existed. The maximum thoretical power P_{max} is calculated as

$$(2)\quad P_{max} = JVA$$

where J is the operating cell current density, V is the operating cell voltage, and A is the active portion of the unit cell area. The various power loss terms contributing to P_{loss} are calculated using standard procedures. Contact resistance has been neglected in the analysis presented here, and current density and illumination are assumed to be uniform over the cells.

In the discussion below, all power terms are calculated for a single cell area to simplify the expressions. (Each power term can be converted to total module power simply by multiplying by the number of cells; the fractional loss F is a ratio and does not change.) The maximum theoretical power available from a single cell area is given by

$$(3)\quad P_{max} = JV(w+w_g)L$$

where w is the active cell width, w_g is the gap width between active cell areas, and L is the cell length, as shown in Figures 1 and 2. The objective is to select design parameters (cell width and grid finger spacing) to minimize the total fractional loss.

SERIES CELLS WITHOUT COLLECTION GRID

In the series configuration without collection grid, the TCO layer only is used for current collection, with no metallic grid added to the surface. The various loss terms are evaluated in the following.

Gap area loss. Cell power loss due to the intercell gap area w_gL is given by

$$(4)\quad P_{gap} = JVw_gL$$

where w_g is the gap width.

TCO resistive losses. The current flow occurs across the cell width parallel to the TCO layer and increases linearly from zero at one cell edge

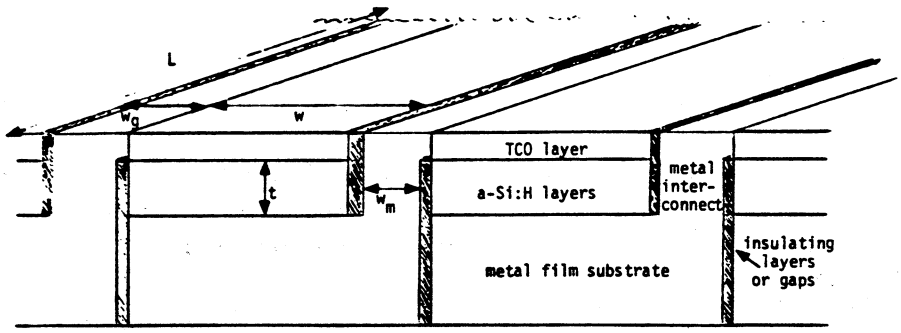

Figure 1. Series Cell Configuration with No Collection Grids

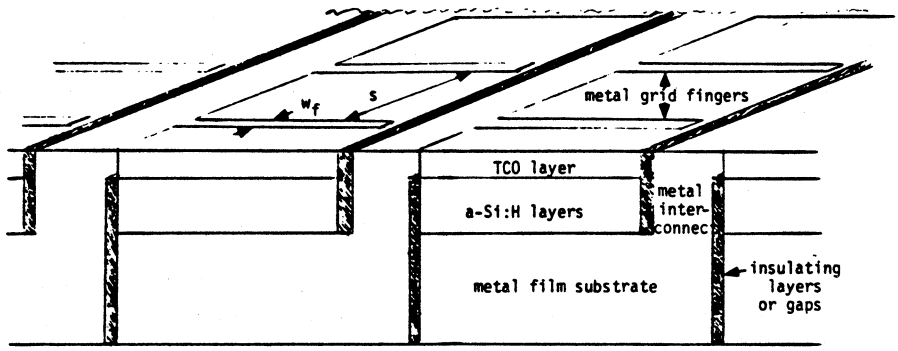

Figure 2. Series Cell Configuration with Metal Collection Grid

SYMBOL	PARAMETER	RANGE	REPRESENTATIVE VALUE
J	cell current density	0.005 - 0.02 A/cm^2	0.015 A/cm^2
V	cell voltage	0.5 - 0.9 V	0.75 V
r_{Si}	bulk resistivity of the a-Si material	1 - 10 ohm-cm	1 ohm-cm*
r_m	bulk resistivity of the metal substrate	10^{-6}- 10^{-7} ohm-cm	10^{-6} ohm-cm
r_{TCO}	sheet resistivity of the TCO layer	10 - 100 ohm_s	10 ohm_s*
r_f	sheet resistivity of the metal grid fingers	0.002 - 0.1 ohm_s	0.01 ohm_s
t	cell thickness	$0.5*10^{-4}$- $5*10^{-4}$ cm	10^{-4} cm
w_g	width of the gap between cells	0.002 - 0.01 cm	0.005 cm*
w_m	width of the metal inter-connect between cells	0.002 - 0.01 cm	0.004 cm
w_f	width of the metal grid fingers	0.001 - 0.01 cm	0.002 cm+

* From Reference (2)

\+ From Reference (3)

Figure 3. Calculation Parameters and Representative Values

to a maximum of JwL at the other cell edge before entering the metal contact. Hence the current in the TCO layer at any distance x across the cell width can be expressed as JxL. The incremental sheet resistance at a distance x is given by $r_{TCO}\,dx/L$ where r_{TCO} is the sheet resistivity of the TCO layer. Thus, the total TCO sheet resistance losses can be integrated as

$$(5)\quad P_{TCO} = \int_0^w (JxL)^2 (r_{TCO}\,dx/L)$$

$$= r_{TCO}\,J^2 w^3 L/3.$$

Bulk resistive losses. The bulk resistance of the a-Si:H layer is given by $r_{Si}t/(wL)$ where r_{Si} is the bulk resistivity of the silicon and t is the thickness. Since the current is JwL, the resulting power loss is

$$(6)\quad P_{bulk} = (JwL)^2 (r_{Si}t/(wL)) = r_{Si}J^2 twL.$$

Metal resistive losses. The metal substrate can be constructed to have very low resistance and hence is assumed to have negligible power losses. The losses in the metal interconnect could be more significant, however, since the interconnect will be made thin so as to reduce the gap size between cells. The resistance of the metal interconnect is $r_m t/(w_m L)$, where r_m is the metal resistivity and w_m is the width of the interconnect, and the current flow is JwL. The resulting power loss is

$$(7)\quad P_{metal} = (JwL)^2 (r_m t/(w_m L)) = r_m J^2 tw^2 L/w_m.$$

Total Loss Fraction. The total loss P_{loss} is simply the sum $P_{gap} + P_{TCO} + P_{bulk} + P_{metal}$. The resulting power loss fraction is then

$$(8)\quad F = P_{loss}/P_{max},$$

which after substitution and algebraic simplification yields

$$(9)\quad F = w_g/(w+w_g) + (r_{TCO}/3)(J/V)w^3/(w+w_g) + r_{Si}(J/V)tw/(w+w_g) + r_m(J/V)t(w^2/w_m)/(w+w_g).$$

The power loss fraction is independent of the cell length and the number of cells in the module.

Approximate Loss Fraction. The fractional loss equation (9) can be approximated assuming that the TCO resistive losses and the cell area losses are much larger than the bulk silicon and metal interconnect resistive losses. The bulk silicon losses are very small because of the thinness of the a-Si cells (t is small); similarly, the metal interconnect losses are very small because of the low resistance even for the narrowest practical gap widths (t and r_m are both small). Present technology permits very small gaps (small gaps are better), so that we may assume $w >> w_g$ and hence $(w+w_g) \cong w$. These approximations permit simplification of equation (9) to yield

$$(10)\quad F \cong w_g/w + (r_{TCO}/3)(J/V)w^2.$$

A computer program was written to compare the approximate equation (10) with equation (9). Using typical cell parameter values as shown in Figure 3, the calculation results were virtually indistinguishable, with the loss terms P_{bulk} and P_{metal} being over three orders of magnitude smaller than P_{gap} and P_{TCO}. The approximation was accurate to three significant digits for gap widths as small as $w_g = 10^{-8}$cm, which is far narrower than that achievable by available manufacturing techniques. Thus, the approximation (10) can be used for any practical calculations of the power loss fraction.

Optimum Cell Width. As the cell width w increases the fractional cell area loss due to the gap decreases, while the TCO resistance losses increase. For a specified value of the gap width w_g (which should be as small as can be practically

achieved in the manufacturing process), the optimum cell width can be determined by setting the derivative dF/dw to zero and solving for w. The resulting optimum cell width is found to be

$$(11)\quad w_{opt} = (1.5Vw_g/(Jr_{TCO}))^{1/3}$$

with fractional losses given by

$$(12)\quad F_{opt} = 1.5w_g/w_{opt}$$
$$= (2.25w_g^2 r_{TCO}J/V)^{1/3}.$$

Thus, the minimum fractional loss is proportional to $w_g^{2/3}$ and $(r_{TCO}J/V)^{1/3}$. This has implications for cell design, i.e., smaller gaps, lower TCO sheet resistivity, and higher cell voltages are preferred.

Representative Calculations. Figure 3 provides a list of typical ranges and representative values for the parameters in the above equations (note that not all parameters shown apply to this no-grid configuration). The resulting fractional power losses are plotted in Figure 4 as a function of the cell width w, assuming a gap width of $w_g = 0.005$ cm. The fractional losses depend on the gap width w_g and the parameter $V/(Jr_{TCO})$; thus, several curves are plotted parametrically in the figure with the representative case being $V/)Jr_{TCO}) = 5$ cm^2. From equation (11) the optimum cell width is $w_{opt} = 0.33$ cm with total fractional power loss of $F_{opt} = 2.2\%$, as shown in the figure. The total fractional loss is not highly sensitive to cell width near the optimum and remains below 5% over the range w = 0.11 cm to w = 0.81 cm. Nevertheless, the acceptable cell widths remain fairly narrow because of the high sheet resistivity of the TCO layer. For example, cell widths of 1 cm result in a fractional loss of about 7.2%. Of course, the thickness of the TCO layer is also subject to optimization with tradeoffs between lower resistivity versus lower transmissivity. Figure 5 plots the optimum values of cell width and total fractional loss as a function of intercellular gap width for different values of $V/(Jr_{TCO})$.

SERIES CELLS WITH COLLECTION GRIDS

In the case of series cells with collection grids, the TCO layer is supplemented by current-carrying metallic fingers. These metallic grid fingers reduce the resistive losses but increase the cell area losses. The various loss terms are summarized below.

Gap Area Loss. Cell area loss due to the intercell gap is the same as before, yielding a power loss given by equation (3).

Metal Finger Area Shading Loss. An additional cell area loss is incurred as a result of shading by the metal grid fingers. The number of grid fingers is $L/(s+w_f)$, where L is the length of the cell, s is the spacing between the metal fingers, and w_f is the width of the fingers. The area of each finger is simply $w_f w$, where w is the width of the cell spanned by the finger. Thus, the area shaded by the fingers is $w_f wL/(s+w_f)$ which yields a power loss of

$$(13)\quad P_{shading} = JVw_f wL/(s+w_f).$$

TCO resistive losses. The TCO resistive losses can be calculated as before, except that now the current flow occurs parallel to the cell length towards the metal fingers. The region starting at the midline between two metal fingers and extending to the finger can be treated as one subcell, with the current flow increasing linearly from 0 at the midline to a maximum of Jws/2 at the grid finger. The current flow at any distance y from the midline is therefore Jwy. The incremental sheet resistance at the distance y from the midline is $r_{TCO}dy/w$. The resistance loss is then integrated from y=0 to y=s/2 and

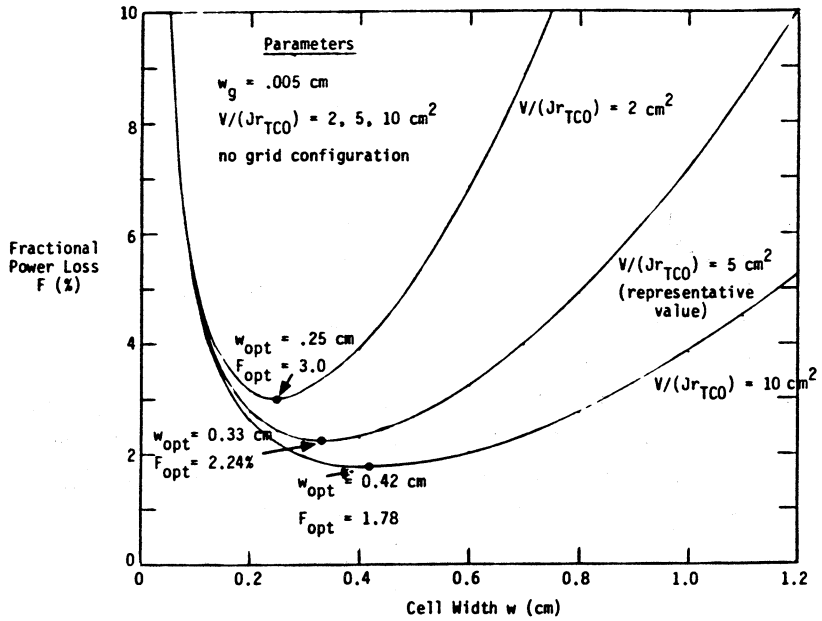

Figure 4. Fractional Loss Versus Cell Width for Parametric Values of $V/(Jr_{TCO})$ (No Grid Configuration)

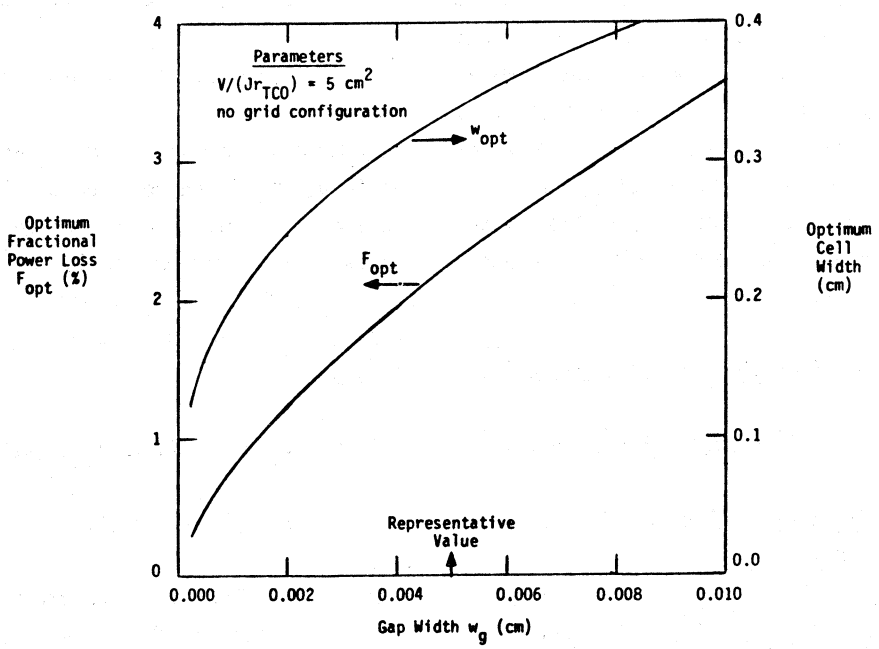

Figure 5. Optimum Values of Cell Width and Fractional Power Loss Versus Gap Width (No Grid Configuration)

multiplied by the number $2L/(s+w_f)$ of subcell areas to yield

$$(14)\ P'_{TCO} = 2L/(s+w_f) \int_0^{s/2} (Jwy)^2 (r_{TCO}\,dy/w)$$

$$= r_{TCO}J^2w(L/12)s^3/(s+w_f).$$

Bulk and Metal Interconnect Losses. The resistive losses in the bulk silicon material and the metal subtrate are similar to those given previously in equations (6) and (7), respectively, except that the current flow is slightly reduced because of finger shading. The current flow is reduced by a factor of $1-w_f/(s+w_f)$ due to shading, so the losses are reduced by the square of this factor, yielding:

$$(15)\ P'_{bulk} = r_{Si}J^2twL(1-w_f/(s+w_f))^2$$

$$(16)\ P'_{metal} = r_mJ^2tw^2L(1-w_f/(s+w_f))^2/w_m.$$

Metal Finger Resistive Losses. The current flow along each metal finger increases linearly from zero to a maximum value of Jws at the intersection with the metal interconnect. Hence, the current flow at a distance z along the finger is Jzs and the incremental resistance is $r_f dz/w_f$, where r_f is the sheet resistivity of the metal fingers. Integrating over $L/(s+w_f)$ fingers yields a power loss of

$$(17)\ P_{finger} = L/(s+w_f) \int_0^w (Jzs)^2 (r_f\,dz/w_f)$$

$$= r_f\,J^2(w^3/w_f)(L/3)s^2/(s+w_f).$$

Total Loss Fraction. The total fractional power loss is given by

$$(18)\ F = (P_{gap} + P_{shading} + P'_{TCO} + P'_{bulk} + P'_{metal} + + P_{finger})/P_{max}$$

$$= w_g/(w+w_g) + w_fw/((w+w_g)(s+w_f)) +$$

$$r_{TCO}(J/V)s^3w/(12(s+w_f)(w+w_g)) +$$

$$r_{Si}(J/V)tw(1-w_f/(s+w_f))^2/(w+w_g) +$$

$$r_m(J/V)t(w^2/w_m)(1-w_f/(s+w_f))^2/(w+w_g) +$$

$$r_f(J/V)s^2w^3/(3w_f(w+w_g)(s+w_f)).$$

Again, the total loss fraction is independent of the cell length and the number of cells in the module.

Approximate Loss Fraction. As described previously, the bulk Si power loss P_{bulk} and the metal interconnect loss P_{metal} are several orders of magnitude smaller in practical designs, since t, r_{Si}, and r_m are very small. Thus, we may approximate

$$(19)\ F \cong (P_{gap}+P_{shading}+P'_{TCO}+P'_{finger})/P_{max}$$

$$= w_g/(w+w_g) + w_fw/((w+w_g)(s+w_f)) +$$

$$r_{TCO}(J/V)s^3w/(12(s+w_f)(w+w_g)) +$$

$$r_f(J/V)s^2w^3/(3w_f(w+w_g)(s+w_f)).$$

In addition, the gap width w_g and the metal finger width w_f should be made as small as practical (the "optimum" is zero, with correspondingly small cell widths and finger spacing), so that we may assume $w >> w_g$ and $s >> w_f$. Hence, under the approximation $(w+w_g) \cong w$ and $(s+w_f) \cong s$, simplification of (19) yields

$$(20)\ F \cong w_g/w + w_f/s + (r_{TCO})(J/V)s^2/12 +$$

$$r_f(J/V)sw^2/(3w_f).$$

Numerical calculation by computer verifies that the approximation (20) is accurate to better than three significant digits (0.1%) for the full range of values given previously in Figure 3.

Optimum Cell Width and Metal Finger Width.

For specified values of the gap width w_g and metal finger width w_f, the optimum values of the cell width w and the metal finger spacing s can be determined by setting the corresponding derivatives dF/dw and dF/ds to zero. This yields two simultaneous cubic equations in w and s:

$$(21)\quad s^3 + 2(r_f/r_{TCO})(w^2/w_f)s^2 - 6w_fV/(r_{TCO}J) = 0$$

$$(22)\quad w^3 - 1.5w_gw_fV/(r_fJs) = 0$$

Solving equation (22) for w in terms of s yields

$$(23)\quad w_{opt} = (1.5w_gw_fV/(r_fJs_{opt}))^{1/3}.$$

Substitution of (23) into (21) and rearranging terms yields

$$(24)\quad s_{opt} = \left|6w_fV/(r_{TCO}J) - \left|(18r_f/w_f)^* (w_gV/J)^2 s_{opt}^4/r_{TCO}^3\right|^{1/3}\right|^{1/3}.$$

This is an implicit equation in s_{opt} since the right hand side contains s_{opt}. However the order of s_{opt} in the right hand side is only $s_{opt}^{4/9}$ so that successive substitution of s_{opt} into (24) converges unless w_f becomes very small (the starting value of s_{opt} must be sufficiently small to give a positive cube root; a good guess is w_{opt} from the no-grid configuration). Thus, solution of equation (24) with several substitutions, followed by evaluation of equation (23), yields the optimum finger spacing s_{opt} and the optimum cell width w_{opt}.

The optimal fractional loss can now be determined by substituting (23) and (24) into (20) yielding:

$$(25)\quad F_{opt} = 1.25w_g/w_{opt} + 1.5w_f/s_{opt}.$$

This is expressed in terms of w_{opt} and s_{opt} to provide a simpler form. Examination of (23), (24), and (25) indicates that smaller gaps w_g, smaller finger widths w_f, smaller r_{TCO}, and smaller (J/V) are preferred.

Representative Calculations. Substitution of the representative parameter values from Figure 3 into equation (24) yields the following implicit equation:

$$(26)\quad s_{opt} = (0.06 - 0.178\, s_{opt}^{4/3})^{1/3}.$$

Successive substitution quickly yields the optimum finger spacing $s_{opt} = 0.29$ (which is close to the optimum cell width given previously for the no-grid configuration). The optimum cell width as given by equation (23) is $w_{opt} = 0.63$ cm, with a total fractional loss of 2.0% from equation (25). The fractional loss remains below 5% for cell widths ranging from w = 0.13 cm to w = 2.00 cm at the same finger spacing, as shown in Figure 6. The optimum cell widths again remain fairly narrow because of rapidly increasing resistive losses in the metal grid fingers as the current flow increases. Figure 7 plots the optimum values of finger spacing, cell width, and total fractional loss as a function of finger width.

DISCUSSION OF RESULTS

The total fractional losses after optimization are about 2% for both the no-grid and grid configurations using achievable values of the gap width and grid finger width. The fractional losses improve with increasing cell voltage to current ratio (V/J), decreasing TCO sheet resistivity (r_{TCO}), and decreasing gap width (w_g). Low values of the TCO sheet resistivity (r_{TCO}) and the gap width (w_g) tend in theory to favor the no-grid configuration, whereas larger TCO resistivity (r_{TCO}), larger gap widths (w_g), and narrow finger widths tend to favor the grid configuration. In general, however, manufacturing considerations will determine the preferred configuration. The

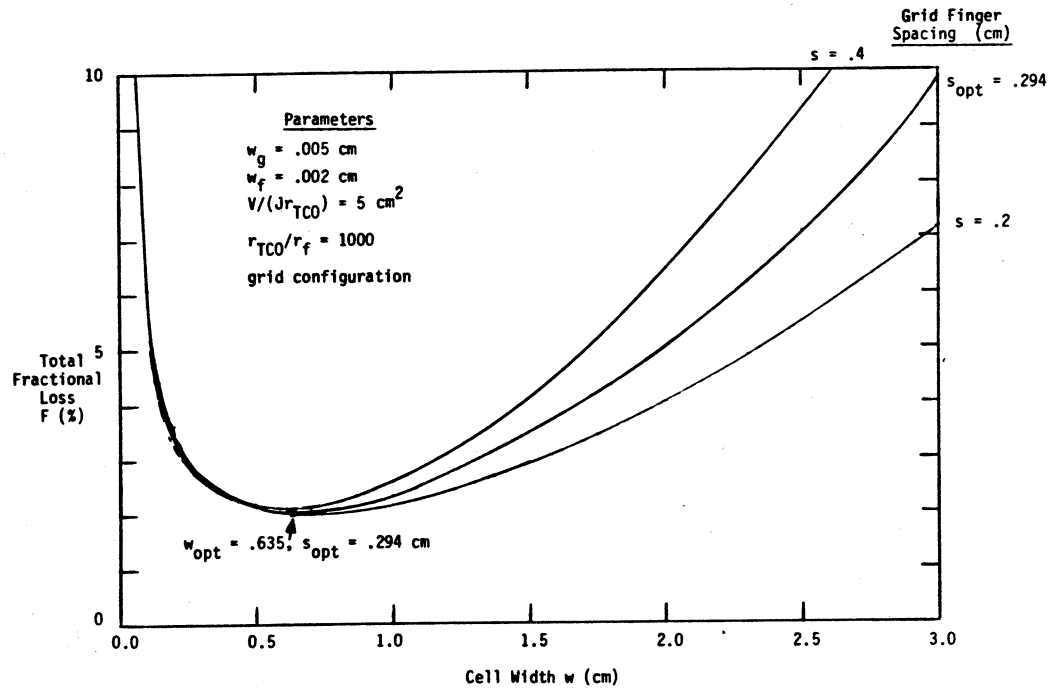

Figure 6. Fractional Power Loss Versus Cell Width and Grid Finger Spacing (Grid Configuration)

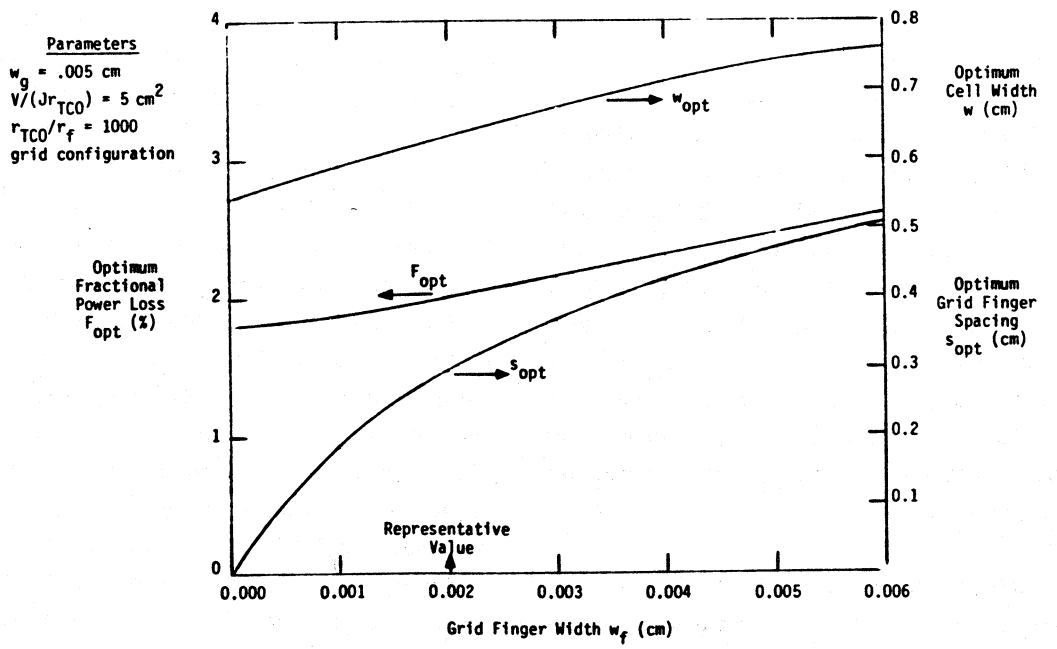

Figure 7. Optimum Values of Cell Width, Grid Finger Spacing, and Fractional Loss Versus Grid Finger Width (Grid Configuration)

configuration with grid permits three to four times larger cell widths, with fewer gaps needed between cells, but also requires grid metallization.

An additional factor which has not been addressed here is cell defects. Pinhole defects which cause short circuits through the cell layer would tend to favor the configuration with no grid, since for the configuration with grid such a defect would short the entire cell. In addition, optimum cell widths would decrease for the grid configuration in order to increase the yield of non-defective cells.

More complicated current collection configurations could also be evaluated using the same techniques. For example, the intercell gap and metal interconnect could be replaced with a parallel metal busbar. Quantitative results are similar except that cell length now becomes a restricted parameter to be optimized.

CONCLUSION

A quantitative methodology has been developed to evaluate power losses resulting from current collection in a-Si:H modules. Analytic expresssions have been derived for optimum cell width and grid spacing as a function of design parameters for series cells with and without metallic collection grids. Current collection losses can be reduced to about 2% using optimized designs with fairly narrow cell widths of less than a centimeter. The methodology can also be used to evaluate other thin film technologies such as CdS.

ACKNOWLEDGEMENTS

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SYMBOL NOTATION

A	= active area of a unit cell area (cm^2)
d	= derivative operator
F	= total fractional power loss resulting from current collection (no units)
F_{opt}	= optimum total fractional power loss (no units)
J	= operating cell current density (A/cm^2)
L	= cell length (cm)
P_{bulk}	= resistive power loss in the bulk a-Si layers (W)
P_{finger}	= resistive power loss in the metal grid P_{gap}=power loss due to the gap between cells (W)
P_{loss}	= total power loss in a unit cell area resulting from current collection resistive and area losses (W)
P_{max}	= maximum theoretically available power from a unit cell area assuming no resistive or cell area losses (W)
P_{metal}	= resistive power loss in the metal interconnect (W)
P_{TCO}	= resistive power loss in the TCO layer (W)
r_f	= sheet resistivity of the metal grid fingers (ohm_s)
r_m	= bulk resistivity of the metal interconnect (ohm-cm)
r_{Si}	= bulk resistivity of the a-Si layers (ohm-cm)
r_{TCO}	= sheet resistivity of the TCO layer (ohm_s)
s	= spacing between metal grid fingers (cm)
s_{opt}	= optimum spacing between grid fingers (cm)
t	= cell thickness (cm)
V	= operating cell voltage (V)
w	= active cell width (cm)
w_f	= width of the metal grid fingers (cm)
w_g	= gap width between cells (cm)
w_m	= width of the metal interconnect between cells (cm)
w_{opt}	= optimum cell width (cm)
x	= distance across cell width (cm)
y	= distance y from the midline between grid fingers (cm)
z	= distance along the metal grid finger (cm)